We claim:

1. An oscillator, comprising:

a plurality of differential inverters configured in a feedback loop to generate an oscillating output signal, each differential inverter including a capacitive trimming network; and

a plurality of digital trimming bits coupled to the capacitive trimming networks for selecting one or more capacitors in each capacitive trimming network, wherein the delay of each differential inverter is simultaneously adjusted in response to the digital trimming bits.

2. The oscillator of claim 1, further comprising:

a comparator coupled to one of the differential inverters that converts the oscillating output signal from a differential signal to a single-ended signal.

3. The oscillator of claim 2, further comprising:

a first divider for dividing the single-ended signal by a factor of 2 to form a first divided signal.

4. The oscillator of claim 3, further comprising:

a second divider for dividing the first divided signal by a factor of 2 to form a second divided signal.

5. The oscillator of claim 4, wherein the second divider is coupled to a reset signal and includes circuitry to synchronize the second divided signal with an external clock signal.

6. The oscillator of claim 1, further comprising:

a bias circuit coupled to the plurality of differential inverters for biasing the differential inverters at a common operating point.

7. The oscillator of claim 1, wherein the differential inverters include a pair of inputs and a pair of outputs, an input stage transistor pair coupled between the pair of inputs and the pair of outputs, and a pair of resistive loads coupled to each output in the pair of outputs.

8. The oscillator of claim 7, wherein the differential inverters further include a pair of base capacitors coupled between the pair of outputs, wherein the base capacitors set a base time delay for signals communicated through the differential inverter.

9. The oscillator of claim 8, wherein the capacitive trimming network is coupled in parallel to the base capacitors between the pair of outputs.

10. The oscillator of claim 9, wherein the differential inverters further include a biasing transistor coupled to an external bias signal and the pair of input transistors.

11. The oscillator of claim 1, wherein the oscillating output signal is used to clock at least one A/D converter and at least one D/A converter in a digital hearing aid system.

12. The oscillator of claim 1, wherein the plurality of differential inverters include at least three differential inverters.

13. The oscillator of claim 2, further comprising:

a bias circuit coupled to the plurality of differential inverters and the comparator for biasing the differential inverters and the comparator at a common operating point.

14. The oscillator of claim 1, wherein the capacitive trimming networks include a plurality of binary weighted capacitors.

15. The oscillator of claim 14, wherein the plurality of binary weighted capacitors are configured in a plurality of binary levels, each binary level including a pair of capacitors and at least one pass transistor, wherein the pass transistor is coupled to one of the digital trimming bits.

16. The oscillator of claim 15, wherein the digital trimming bits turn on and off the pass transistors at each of the binary levels in order to selectively connect the pair of capacitors in each of the binary levels to the differential inverters.

17. The oscillator of claim 16, wherein the plurality of binary levels includes at least five levels.

18. The oscillator of claim 16, wherein the capacitive trimming networks are coupled to an output stage of the differential inverters.

19. The oscillator of claim 7, wherein the pair of resistive loads and the input stage transistor pair are manufactured from a common semiconductor process.

20. The oscillator of claim 19, wherein the pair of resistive loads are made of non-salicided polysilicon.

21. The oscillator of claim 7, wherein the input stage transistor pair are NMOS devices.

22. The oscillator of claim 1, wherein the frequency of the oscillating output signal is varied by selecting one or more of the digital trimming bits.

23. The oscillator of claim 13, wherein the bias circuit is a constant transconductance bias circuit.

24. The oscillator of claim 22, wherein the frequency of the oscillating output signal can be varied by about +/- 2.5% from a nominal frequency value via the digital trimming bits.

25. A differential inverter, comprising:

a pair of inputs and a pair of outputs;

an input stage transistor pair coupled between the pair of inputs and the pair of outputs;

a pair of resistive loads coupled to the pair of outputs; and

a digital capacitive trimming network coupled between the pair of outputs for adjusting the delay of the differential inverter.

26. The differential inverter of claim 25, further comprising:

a plurality of digital trimming bits coupled to the capacitive trimming network, wherein each of the digital trimming bits selects one or more capacitors in the capacitive trimming network to adjust the delay of the differential inverter.

27. The differential inverter of claim 25, further comprising:

a pair of base capacitors coupled between the pair of outputs, wherein the base capacitors set a base time delay for signals communicated through the differential inverter.

28. The differential inverter of claim 27, wherein the pair of base capacitors and the capacitive trimming network are connected in parallel.

29. The differential inverter of claim 25, further comprising:

a biasing transistor coupled to an external bias signal and the input stage transistor pair.

30. The differential inverter of claim 25, wherein the capacitive trimming network includes a plurality of binary weighted capacitors.

31. The differential inverter of claim 30, wherein the plurality of binary weighted capacitors are configured in a plurality of binary levels, each binary level including a pair of capacitors and at least one pass transistor, wherein the pass transistor for each level is coupled to one of a plurality of digital trimming bits.

32. The differential inverter of claim 31, wherein the digital trimming bits turn on and off the pass transistors at each of the binary levels in order to selectively connect the pair of capacitors in each of the binary levels to the pair of outputs.

33. The differential inverter of claim 32, wherein the plurality of binary levels includes at least five levels.

34. The differential inverter of claim 25, wherein the pair of resistive loads and the input stage transistor pair are manufactured from a common semiconductor process.

35. The differential inverter of claim 34, wherein the pair of resistive loads are made of non-salicided polysilicon.

36. A digital hearing aid system, comprising:

at least one microphone for receiving a sound signal;

an analog to digital (A/D) converter for converting the sound signal into a digital sound signal;

a digital sound processor for processing the digital sound signal;

a digital to analog (D/A) converter for converting the processed digital sound signal into an analog sound signal;

a speaker for transmitting the analog sound signal; and

a precision, low jitter oscillator circuit for generating an adjustable clock signal that is coupled to the A/D converter, the D/A converter, and the digital sound processor, wherein the precision, low jitter oscillator circuit includes a plurality of differential inverters configured in a feedback loop, each differential inverter including a capacitive trimming network for adjusting the clock signal and a resistive load for minimizing jitter.

37. A precision, low jitter oscillator for generating an adjustable clock signal, comprising:

a plurality of differential inverters configured in a feedback loop to generate an oscillating clock signal, each differential inverter including a capacitive trimming network that is coupled to a plurality of digital trimming bits

for selecting one or more capacitors in each of the capacitive trimming networks to thereby adjust the frequency of the oscillating clock signal.

38. The precision, low jitter oscillator of claim 37, wherein each of the differential inverters includes and input stage and an output stage, and a resistive load coupled to the output stage for minimizing jitter in the oscillating clock signal.